ABSTRACT OF THE DISCLOSURE

A semiconductor storage device with high soft-error immunity is obtained. A semiconductor storage device has SRAM memory cells. NMOS transistors (Q1, Q4) are driver transistors, NMOS transistors (Q3, Q6) are access transistors, and PMOS transistors (Q2, Q5) are load transistors. An NMOS transistor (Q7) is a transistor for adding a resistance. The NMOS transistor (Q7) has its gate connected to a power supply (1). The NMOS transistor (Q7) has one of its source and drain connected to a storage node (ND1) and the other connected to the gates of the NMOS transistor (Q4) and the PMOS transistor (Q5). The resistance between the source and drain of the NMOS transistor (Q7) can be adjusted with the gate length, the gate width, the source/drain impurity concentration, etc., which is, for example, about several tens of kilohms (kΩ).